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(54) Title: METHOD FOR MANUFACTURING FLAT PANEL DISPLAY SUBSTRATES

(57) Abstract: A system an method for generating thin film transistors, the system employing a non-excimer laser beam interacting with amorphous silicon disposed on a substrate surface to form mutually spaced apart silicon crystals on the surface.

METHOD FOR MANUFACTURING FLAT PANEL DISPLAY SUBSTRATES

CROSS REFERENCE TO RELATED APPLICATION

[0001] This application claims the benefit of U.S. Provisional Patent Application No. 60/358,734, filed February 25, 2002, the disclosure of which is incorporated by reference in its entirety.

FIELD OF THE INVENTION

[0002] The present invention generally relates to systems and methods operative to heat selected locations on thin film materials, and more particularly systems and methods operative to induce a phase change in a material, for example to form crystalline silicon deposits on substrates that subsequently can be incorporated into transistor arrays found on electronic devices, such as flat panel displays.

BACKGROUND OF THE INVENTION

[0003] Thin film transistors are used in a variety of applications, including flat display screens. In some applications, it is desirable to construct thin film transistors from crystallized silicon.

[0004] One way to produce crystallized silicon is to deposit a layer of amorphous silicon on a substrate, and then anneal the amorphous silicon using laser energy to heat the amorphous silicon, for example using laser energy provided by excimer lasers.

SUMMARY OF INVENTION

[0005] The present invention seeks to provide improved systems and methods for delivering laser energy to heat a substrate at selected non-contiguous locations, but substantially not heat other locations.

[0006] The present invention seeks to provide improve systems and method to induce a localized change in a physical property of a substrate at a multiplicity of non-contiguous locations.

[0007] The present invention seeks to provide improved systems and methods for forming silicon crystals on substrates.

[0008] The present invention further seeks to provide improved systems and methods for annealing amorphous silicon.

[0009] The present invention further seeks to provide an improved substrate for use in fabricating flat panel displays, the substrate manufactured by forming a multiplicity of silicon crystals at non-contiguous locations.

[0010] In accordance with a general aspect of the present invention, a plurality of laser beams are employed to heat a semiconductor precursor, for example non-crystallized silicon, at selected non-contiguous locations on a substrate surface.

[0011] In accordance with a general aspect of the present invention, a laser beam is employed to interact with non-crystallized silicon at non-contiguous locations on a substrate surface to form silicon crystals thereat.

[0012] In accordance with another general aspect of the invention, a non-eximer laser is employed to interact with non-crystallized silicon, such as amorphous silicon, to crystallize silicon at non-contiguous locations.

[0013] In accordance with another general aspect of the invention, a pulsed laser beam having a pulse repetition rate of greater than 5 KHz is employed to interact with non-crystallized silicon, such as amorphous silicon, to crystallize the silicon at non-contiguous locations.

[0014] In accordance with another general aspect of the invention, a pulsed laser outputting a pulsed laser beam having a total average power of less than 50W is employed to interact with non-crystallized silicon, such as amorphous silicon, to crystallize the silicon at non-contiguous locations.

[0015] In accordance with another general aspect of the invention, a plurality of laser beams is employed to interact with non-crystallized silicon, such as amorphous silicon, disposed on a substrate surface to simultaneously form mutually

spaced apart silicon crystals on the surface. Optionally the plurality of laser beams is formed from a non-excimer laser beam, or from a laser beam having a total average power of less than 50W, or from a laser beam having a pulse repetition rate of greater than 5 KHz, or from any suitable combination of the foregoing.

[0016] In accordance with another general aspect of the invention, a laser beam is divided into a plurality of sub-beams, each of which is directed to impinge on a positioner operative to selectively position a sub-beam so that it impinges at, or near, a selected location of non-crystallized silicon disposed on a substrate surface, such that a silicon crystal is formed at each selected location. Optionally the laser beam is provided by a non-excimer laser, or it is provided by a laser outputting a pulsed laser beam having a total average power of less than 50W, or it is a pulsed laser beam having a pulse repetition rate of greater than 5 KHz, or any suitable combination of the foregoing. In accordance with an embodiment of the invention, the pitch between the sub-beams is adjustable.

[0017] In accordance with an embodiment of the invention, there is provided a method for fabricating a substrate having thin film transistors, comprising providing a substrate having silicon deposited on a surface thereof and simultaneously delivering a plurality of laser beams to a first plurality of non-contiguous locations on the surface to induce said silicon to undergo a change in a physical state, for example crystallization by melting and subsequent cooling, at said non-contiguous locations, and not to undergo a change in physical state at other locations. This method is applicable, for example, to the formation of flat panel displays such as LED displays.

[0018] In accordance with another embodiment of the invention, there is provided a method for fabricating a substrate having transistors, comprising providing a substrate comprising silicon annealing the silicon at a plurality of non-contiguous locations, and removing the silicon without masking, at least at locations other than at the non-contiguous

locations. The some crystallized silicon at the non-contiguous locations may also be removed.

BRIEF DESCRIPTION OF DRAWINGS

[0019] The present invention will be understood and appreciated more fully from the following detailed description, taken in conjunction with the drawings in which:

[0020] Fig. 1 is a simplified pictorial illustration of a system for selectively heating a substrate in accordance with an embodiment of the invention;

[0021] Fig. 2 is a simplified flow diagram of a method for forming thin film transistors on a substrate employing the system of Fig. 1;

[0022] Fig. 3 is a simplified pictorial illustration of a system for selectively heating a substrate in accordance with another embodiment of the invention;

[0023] Fig. 4 is a simplified diagram of a control signal employed in the system of Fig. 3;

[0024] Fig. 5 is a simplified schematic illustrations of acoustic waves, and their affect on laser beam pulses, employed in the system of Fig. 3.

DETAILED DESCRIPTION

[0025] Reference is made to Figure 1, which is a simplified pictorial illustration of a system 10 for selectively heating a substrate, for example to form silicon crystals on a substrate 12, such as polycrystalline silicon on a glass substrate of the type employed in flat panel displays, in accordance with an embodiment of the invention. System 10 includes a laser 14, controlled by a laser control unit 16. In the embodiment of the invention seen in Fig. 1, laser 14 is associated with a pulse supply unit 18, such as a Q-switch, to output a pulsed laser beam 20. In the embodiment of Fig. 1, beam 20 is first passed through a frequency converter 21, such as one or more non-linear crystals, and then through optics 22, such as beam shaping optics, to impinge on a beam splitter 24 operative to split beam 20 into a plurality of sub-beams 26. It is noted that laser 14

may be operative to directly output a laser beam having a desired frequency such that the necessity of frequency converter 21 is obviated. It is further noted that that sub-beams 26 may be provided by any suitable means, for example by an array of laser diodes.

[0026] In the embodiment seen in Fig. 1, each of the sub-beams 26 exits beam splitter 24 at a suitable angular orientation so as to impinge on a reflector 28 operative to direct the beams to a given location on the surface of substrate 12. Reflector 28 may comprise, for example, an array of fixed or adjustable directional reflecting elements (not shown) to provide further directional control for each sub-beams 26. Optionally, angle expanding optics (not shown) is interposed between the beam splitter 24 and reflector 28. It is noted that in Fig. 1 a reduced number of beams and exaggerated angles are shown for reasons of simplicity and ease of understanding the general concepts underlying the invention.

[0027] Downstream of the reflector 28, sub beams are passed through additional optics 30, including, for example a focusing lens and a telecentric imaging lens, to impinge on the surface of a semiconductor precursor layer 32, such as a thin film of amorphous silicon, overlaying substrate 12. Optics 30 may comprise optics treating all of the sub-beams 26 as a group as seen, or an array of optics independently treating each of sub-beams 26.

[0028] At each location 34 where a sub-beam 26 impinges on semiconductor precursor layer 32, the semiconductor precursor layer 32 is heated, as shown diagrammatically by heat waves 36. The heating takes place at locations 34 however the precursor layer substantially is not heated elsewhere. That is to say, at locations other than locations 34, no melting of the semiconductor precursor layer 32 occurs. Moreover, in flat panel display construction, heating at locations 34 does not melt the glass substrate or change its optical properties.

[0029] When the semiconductor precursor layer is, for example, formed of amorphous silicon, the process of heating and subsequent cooling forms a silicon crystal 38 at each location 34 impinged upon by a sub-beam 26. This process of forming a

crystal 38 by heating and cooling is called annealing. In accordance with an embodiment of the invention, each of sub-beams 26 impinges on the semiconductor precursor layer 32 at non-contiguous, or mutually spaced apart, locations 34, such that each resulting crystal 38 is mutually spaced apart from other crystals 38 that are formed in semiconductor precursor layer 32.

[0030] It is a particular feature of the present invention that the laser 14 employed to selectively anneal layer 32 is a relatively low power pulsed laser, such as a non-excimer pulsed laser. Such lasers typically have an average power output that is substantially less than a typical excimer laser employed in industrial applications such as semiconductor or flat panel display fabrication. Suitable lasers have, for example, an average power output of less than about 50W, and typically in the order of about 5-15W. Moreover, suitable Q-switch lasers operate at a pulse repetition rate of greater than about 5KW.

[0031] Consequently, the process of selectively annealing semiconductor precursor layer 32, in accordance with an embodiment of the invention, employs a beam director operative to direct laser beams 26 substantially to those non-contiguous locations 34 whereat it is desired to form a crystal 38, and not to other locations.

[0032] Typically, crystals 38 are formed substantially only at those locations where transistors are needed in an electrical device to be manufactured from substrate 12, and not at other locations. Such crystals generally occupy between 0.1% - 5%, of the surface of substrate 12, and typically about 1% of the surface.

[0033] The inventors have found that a frequency converted Q-switched laser, outputting a beam which is the product of third harmonic generation of a Nd:YAG solid state laser, is suitable for use in system 10. Suitable lasers 14 emit pulses at a pulse repetition rate in the range of 5 - 100 KHz, with a duty cycle in the range of 1:100 - 1:10,000. The average power associated with such suitable lasers is less than about 50W. Typically average power is in the range of between 5W to 10W, although the power of suitable lasers currently under development may reach

as high as 15W or higher. A commercially available laser meeting these requirements, and including both laser 14 and frequency converter 21 as an integral unit, is the AVIA™ laser available from Coherent, Inc. of California U.S.A.. The AVIA™ laser outputs an approximately 7.5W average power pulsed frequency converted UV laser beam at 355nm. The beam has a repetition rate of about 30KHz, and a pulse width of about 100 nsec. It is appreciated that any other suitable solid state, gas or semiconductor pulsed non-excimer laser may be used. Likewise, other suitable forms of frequency conversion, other than harmonic generation, may be employed.

[0034] In the embodiment seen in Fig. 1, optics 22 are employed to suitably expand and shape beam 20 so that it impinges on beam splitter 24 so as to be divided into a plurality of sub-beams 26, each of which is emitted so as to impinge on the surface of substrate 12 at a given location. Optics 22 may include a single optical component or multiple optical components. The optical components may be any combination of spherical, cylindrical, aspherical, holographic diffractive, or other suitable optical components as known in the art of optical design.

[0035] Beam-splitter 24 may be any suitable beam splitter, such as, for example, an array of suitable diffractive elements. In accordance with an embodiment of the invention, beam 20 is divided into between 80 - 120 sub beams. It is noted that a lesser number of beams is shown for simplicity of illustration. Because a typical electronic device may include several million thin film transistors, while typically up to only up to about 120 non-contiguous locations 34 are addressable at a given time, a displacer (not shown) is provided to move substrate 12 and system 10 relative to each other, as known in the art. The displacer enables crystals 38 to be formed on other parts of layer 32.

[0036] The choice of the number of sub-beams 26 into which beam 20 is to be divided is a matter of design choice. The choice is functionally related the desired energy density at which a sub-beam is to be delivered to each of locations 34. Thus, in order to anneal a location 34 of about 20 μm diameter

with a sub-beam 26 having an energy density of about 500 mJ/cm^2, a laser 14 emitting a pulsed beam of about 0.25 mJ would be divided into about 100 sub-beams 26.

[0037] The inventors believe that when system 10 is used to anneal amorphous silicon, the use of a plurality of sub-beams results in an improved crystalline structure of crystals 38 at non-contiguous locations 34, compared to systems which apply laser beams to anneal layer 32 substantially in its entirety. When sub-beams 26 are configured and operative to completely melt layer 32 throughout a relatively small region, generally at a location 34, lateral crystal growth is stimulated at a location 34. In the crystallization of amorphous silicon into poly-silicon, such lateral growth produces relatively large grain polycrystalline silicon. The phenomenon of lateral growth can be facilitated by optimizing the melt-down of layer 32 at each non-contiguous location 34, such that at a non-contiguous location 34 layer 32 is completely and uniformly melted. The melt-down of layer 32 can be optimized by suitably shaping sub-beams 26, for example through the suitable optical design, including the design of optics 22, beam splitter 24, and additional optics 30.

[0038] In order to ensure uniformity in the formation of crystals 38, and in order to stimulate desirable lateral growth, it is necessary to ensure that a precise and uniform dose of laser energy is delivered to each of locations 34. Uniformity among beams may be accomplished, for example, with an attenuator (not shown), such as a polarizing beam cube, associated with each sub-beam 26. Dose control for all of the beams may be accomplished by changing the pulse repetition rate of laser 14, for example by controlling pulse supply unit 18.

[0039] Moreover, sub-beams 26 may be directed to anneal silicon at non-contiguous locations 34 so as to form thereat silicon crystals having a desired shape. This may be accomplished by controlling the positioning of sub-beams 26, or by suitable displacement of substrate 12 during annealing. The formation of silicon crystals having a desired shape is advantageous, or example, inasmuch as silicon may be removed without masking. Because of differences in the rate of removal

of annealed and non-annealed silicon, silicon removal may be effected, such as by etching, so as to leave deposits of silicon crystals which are appropriately shaped and ready for subsequent operations in the fabrication of transistors.

[0040] Reference is now made to Fig. 2 which is a simplified flow diagram of a method for forming thin film transistors on a substrate employing the system of Fig. 1. The method seen in Fig. 2 commences with generating a laser beam, for example by means of a Q-switched solid state laser in combination with one or more non-linear crystals suitable for third harmonic generation. The beam is passed through a suitable beam splitter operative to divide the laser beam into a plurality of sub-beams.

[0041] In accordance with an embodiment of the invention, at least some of the sub-beams are each delivered to impinge on the surface of a substrate to address a respective non-contiguous locations on the substrate. The substrate includes a semiconductor precursor layer, such as a thin film of amorphous silicon, which is deposited, for example, on glass or other suitable substrate. Each of the locations addressed by a sub beam is at least partially separated from locations addressed by other sub-beams.

[0042] The sub-beams are delivered to their respective locations at an energy density, and for an amount of time or number of pulses, sufficient to provide an energy dose operative to heat the semiconductor precursor at the respective locations of impingement. The dose is optimized to be sufficient to thoroughly melt the semiconductor precursor at a location impinged upon by a sub-beam, but not so much as to adversely affect the substrate on which the semiconductor precursor is deposited or to cause a melting of the semiconductor precursor outside of a location having a desired shape.

[0043] After heating the semiconductor precursor, the substrate is cooled. This annealing process results in the growth of a crystal at each location addressed by a sub-beam. The process of delivering a sub-beam, heating the semiconductor substrate and then cooling is repeated until all of a multiplicity of desired locations on a workpiece are suitably

annealed. In an embodiment of the invention, the desired locations at which are those locations at which it is desired to form a transistor, or other semiconductor component.

[0044] After annealing each of the locations at which it is desired to form a transistor or other semiconductor component, other non-annealed portions of the semiconductor precursor, for example those portions of amorphous silicon that have not been state changed into crystallized poly-silicon, are removed. Removal may be, for example by way of etching or any other suitable removal technique.

[0045] The remaining portions of semiconductor precursor are thus, for example, poly-silicon crystals each of which is located at a location corresponding to a location where transistors, or other semiconductor components, are to be deposited. The remaining crystals are doped, and otherwise treated, and then electrically interconnected in order to form an array of transistors, or other semiconductor components, deposited on the workpiece. The workpiece may then be fabricated into a desired electronic device, for example a flat panel display, by appropriate additional electronic device fabrication steps.

[0046] The system described hereinabove with reference to Figs. 1 and 2 is operative to selectively anneal layer 32 in a fixed pattern. The pattern is functionally related to a pattern of beams output by beam splitting element 24, or by a spatial arrangement of directional reflecting elements in reflector 28, for example a two dimensional mapping assembly receiving a plurality of beams output in a plane, as described in greater detail in copending U.S. patent application 10/170,212 to Gross et al. for a Multiple Beam Micro-Machining System and Method, the disclosure of which is incorporated herein by reference in its entirety.

[0047] It is noted, however, that in the fabrication of thin film transistors the pitch and layout of transistors making up an electronic device may not be constant and fixed between different designs of electronic devices. It may be desirable to move a beam during annealing in order to generate a crystal having a desired shape. Moreover, the pitch and layout may not

be constant and fixed between regions in the same electronic device.

[0048] Reference is now made to Fig. 3 which is a simplified pictorial illustration of a system 110 for forming silicon crystals on a substrate 112, such as polycrystalline silicon crystals on a glass substrate of the type employed in flat panel displays, in accordance with another embodiment of the present invention. System 110 seen in Fig. 3 is adapted, *inter alia*, to accommodate the formation of crystalline semiconductor deposits at different pitches and layouts, as may be selected from time to time. Moreover, system 110 is operative to accommodate different pitches and layouts within the same electronic device, as well as different pitches and layouts that may characterize the respective designs of different electronic devices. Additionally, system 110 may be operative to anneal amorphous silicon such that each of the resulting crystals has a selectable shape. This is accomplished by controlling the positioning laser beams employed to anneal silicon deposited on substrate 112.

[0049] System 110 includes a laser 114, controlled by a laser control unit 116. In the embodiment of the invention seen in Fig. 1, laser 114 is associated with a pulse supply unit 118, such as a Q-switch, to output a pulsed laser beam 120. In the embodiment of Fig. 3, beam 120 is first passed through a frequency converter 121, such as one or more non-linear crystals, and then through optics 122, such as beam shaping optics, to impinge on a beam splitter 124 operative to split beam 120 into a plurality of sub-beams 126. It is noted that laser 114 may be operative to directly output a laser beam having a desired frequency such that the necessity of frequency converter 121 is obviated. It is further noted that sub-beams 126 may be provided by any suitable means, for example by an array of laser diodes.

[0050] It is a feature of the embodiment seen in Fig. 3 that the respective locations at which sub-beams 126 impinge on the surface of substrate are selectable and controllable. Thus, each of the sub-beams 126 exits beam splitter 124 at a suitable angular orientation so as to impinge on a first reflector 128

operative to direct each of sub-beams 126 to a corresponding directionally controllable deflector 150 in an array 152 of deflectors 150. In accordance with an embodiment of the invention, first reflector comprises an array of reflector elements arranged as a two dimensional mapping assembly, for example as described in greater detail in copending U.S. patent application 10/170,212 to Gross et al. for a Multiple Beam Micro-Machining System and Method, the disclosure of which is incorporated herein by reference in its entirety.

[0051] In the embodiment seen in Fig. 3, first reflector 128 comprises a plurality of directional reflecting elements 129, each of which is mapped to a corresponding directionally controllable reflector 150 in an array 152 of directionally controllable reflectors 150.

[0052] In the embodiment seen in Fig. 3, each directionally controllable reflector 150 comprises a mirror 160, or other suitable reflective element, mounted on a positioner assembly 162 comprising a base 164, a mirror support 166, a least one selectable actuator 168 (three are shown assembled in a starlike arrangement), and a biasing spring (not shown) beneath mirror 160. Each of the selectable actuators 168 is, for example, a piezoelectric actuator, such as a TORQUE-BLOCK™ actuator available from Marco Systemanalyse und Entwicklung GmbH of Germany, independently providing an up and down positioning as indicated by arrows 172 so as to selectively position mirror 160 in a desired spatial orientation to receive a sub-beam 126 and direct the sub-beam to a desired location on the surface of substrate 112.

[0053] Although in the embodiment shown in Fig. 3 directionally controllable reflector 150 employs a piezoelectric actuator, it is appreciated that any other suitable actuator for selectably orienting mirror 160 may be used. These may include, for example, any a suitable linear motor, MEMS or MOEMS device, or a Digital Micromirror Device™ available from Texas Instruments Corporation of Texas.

[0054] Each of the actuators 168 is operatively connected to a servo controller 174 which in turn is operatively connected to

and controlled by a computer controller 176. A computer file, such as a CAM data file 178, containing the appropriate layout of locations at which a silicon crystal is to be formed on substrate 112 is input into the computer controller. The CAM data file 178 is used to determine the pitch and layout of locations to be annealed, and respective spatial orientation required of each mirror 160. The computer controller suitably instructs the servo controller to adjust the respective orientations of mirrors 160 in array 152.

[0055] In accordance with an embodiment of the invention, beam splitter 124 is a variable deflector assembly such as an acousto-optical deflector (AOD). A suitable beam splitter is described in greater detail in copending U.S. patent application 60/387,911 to Gross and Kotler. for a Dynamic, Multi-Pass, Acousto-Optic Beam Splitter & Deflector (BSD), the disclosure of which is incorporated herein by reference in its entirety. As seen in Fig. 3, beam-splitter 124 includes a transducer 180 and a translucent crystal member 182 formed of Quartz or other suitable crystalline material.

[0056] Transducer 180 receives a control signal 184 and generates an acoustic wave 186, seen as a collection of planar waves, that propagates through crystal member 182. Control signal 184 preferably is an RF signal provided by an RF modulator 188, preferably driven by a direct digital synthesizer (DDS) 190, or other suitable signal generator, for example a voltage controlled oscillator (VCO). Control of the control signal may be provided, for example, by the computer controller 176, in response to the CAM data file 178, and optionally other inputs, such as sensed inputs.

[0057] As known in the art, the presence of an acoustic wave 182 in crystal member 182 at the instant beam 120 impinges thereon causes beam 120 to be deflected at an angle θ which is a function of the frequency f of acoustic wave 186 according to the formula:

$$\theta_n = \frac{\Delta f_n \times \lambda}{\upsilon_s}$$

[0058] Where:

$$\Delta f_n = f_n - f_0$$

λ = wavelength of beam 14

υ_s = speed of sound in the crystal of AOD 20

[0059] Control signal 184 may be provided selectively so as to cause acoustic wave 186 to propagate uniformly through crystal member 182, or alternatively so as to cause acoustic wave 182 to propagate at a plurality of different frequencies. In an embodiment of the invention, the acoustic wave is formed so that it has a plurality of different frequencies such that a different frequency wave is formed in a different localized region in crystal member 182. Thus when acoustic wave 186 is non-uniformly propagated through crystal member 182, beam 120 is segmented sub-beams 126, each of which is deflected at an angle θ_n which is a function of an acoustic wave frequency of acoustic wave 186 at a localized region in crystal member 182 at the instant pulses comprising beam 120 impinge on the crystal member 182.

[0060] Reference is now made to Fig. 4 which is a simplified diagram of a control signal 184 employed in the system of Fig. 3, and to Fig. 5 which is a simplified schematic illustrations of acoustic waves 186, and their affect on laser beam 120, employed in the system of Fig. 3. Thus as seen in Fig. 6, a control signal 184 has several segments 192, each of which has a corresponding frequency. As seen in Fig. 7, the acoustic wave 186 interacts with beam 120 passing through crystal member 182 to divide beam 120 into a plurality of sub-beams 126 as a function of the quantity of segments 192 of acoustic wave 186, and to deflect a sub-beam 126 at an angle which is a function of the frequency of acoustic wave 186 at each of segments 192. Thus segmentation of beam 120 into sub-beams is a function of the frequencies in acoustic wave 186, which is variable, and is independent of any permanent physical segmentation in crystal member 182.

[0061] It is noted the use of a variable deflector assembly, such beam splitter 124 in Fig. 3, enables control of the quantity of sub-beams 126 used in the annealing process. Thus, one way to adjust the dosage of laser energy in a beam supplied

to anneal silicon is to control beam splitter 124 so that beam 120 is divided into a greater or lesser number of sub-beams 126. Additionally, the precise dosage supplied to each annealing location can be controlled by the acoustic power introduced for beam deflection, as is known in the art, for example by changing the fluence of a sub-beam 126. Additional aspects of a system and method for micro-machining a substrate with a plurality of simultaneous laser beams are described in detail in copending U.S. patent application 10/170,212 to Gross et al. for a Multiple Beam Micro-Machining System and Method, the disclosure of which is incorporated herein by reference in its entirety.

[0062] Precision energy control is very important for lateral crystal growth. In the crystallization of amorphous silicon into poly-silicon by lateral growth in general and super lateral growth in particular, precise temperature of the silicon during melt-down is extremely important and may affects the quality of crystalline silicon. Thus, for example, melt-down may proceed by ramping up the energy in a beam during melt-down, or by providing an initial blast of high energy followed on by a beam having a lesser energy density. The energy density of a beam may be controlled as a function of the quantity of sub-beams 126 formed from a beam 120 output by laser 114.

[0063] Returning to Fig. 3, it is seen that angle expanding optics 127 are interposed between the beam splitter 124 and first reflector 128. It is noted that upon exit from beam splitter 124, when configured as an acousto-optical deflector, the respective angles of sub-beams 126 typically are very small, and much smaller than the angles depicted in the figure. It is noted that in Fig. 3 a reduced number of beams and exaggerated angles are shown for reasons of simplicity and ease of understanding the general concepts underlying the invention. Typically, the quantity of sub-beams will be the same as, or similar to the number of directionally controllable reflectors 150 in array 152, and the angles of divergence will be considerably smaller, however when a higher energy density in beams 126 is desired, a smaller number of beams may be output from beam splitter 126.

[0064] Downstream of the array 152, sub beams are passed through additional optics 130, including, for example a focusing lens and a telecentric imaging lens, to impinge on the surface of a semiconductor precursor layer 132, such as a thin film of amorphous silicon, overlaying substrate 12. In accordance with an embodiment of the invention, a controllable focusing lens may be provided for each sub beam 126 and the need for a telecentric imaging lens operative to simultaneously image all of beams 126 is obviated.

[0065] At each location 34 where a sub-beam 126 impinges on semiconductor precursor layer 132, the semiconductor precursor layer 132 is heated, as shown diagrammatically by heat waves 36. When the semiconductor precursor layer is, for example, formed of amorphous silicon, the process of heating and subsequent cooling forms a silicon crystal 38 (Fig. 1) at each location 34 impinged upon by a sub-beam 126. This process of forming a crystal 38 (Fig. 1) by heating and cooling is called annealing. In accordance with an embodiment of the invention, each of sub-beams 126 impinges on the semiconductor precursor layer 132 at mutually spaced apart locations 34, such that each resulting crystal 38 is mutually spaced apart from other crystals 38.

[0066] It is a particular feature of the present invention that the laser 114 employed to selectively anneal layer 32 is a non-excimer pulsed laser. Such lasers typically have a power output that is substantially less than a typical excimer laser employed in industrial applications such as semiconductor or flat panel display fabrication. Consequently, the process of selectively annealing semiconductor precursor layer 132, in accordance with an embodiment of the invention, directs laser beams substantially to those locations 34 where it is desired to form a crystal 38, and not to other locations.

[0067] Moreover, directionally controllable reflectors may be employed to slightly move a sub-beam 126 between subsequent laser beam pulses to address a neighboring location that is near to or in contact with a previously addressed location 34. This process may be employed to grow larger crystals 38 as necessary, or to form crystals having a desired shape. Forming crystals having a desired shape may be useful, for example, in a maskless

production operation inasmuch as amorphous silicon can be removed, e.g. by etching, at a faster rate than crystalline silicon.

[0068] Typically, crystals 38 are formed substantially only at those locations where transistors are needed in an electrical device to be manufactured from substrate 112, and not at other locations. Such crystals generally occupy between 0.1% - 5%, of the surface of substrate 112, and typically about 1% of the surface.

[0069] Other aspects of the embodiment seen in Fig. 3 are generally as described hereinabove with respect to Fig. 1, and its use in the generation of thin film transistors and electronic devices is generally as described hereinabove with reference to Fig. 2.

[0070] It is appreciated by persons skilled in the art that the present invention is not limited by what has been particularly shown and described hereinabove. Rather the present invention includes modifications and variations thereof which would occur to a person of skill in the art upon reading the foregoing description and which are not in the prior art.

What is claimed is:

1. A method for fabricating a substrate having thin film transistors, comprising:

providing a substrate having a semiconductor precursor deposited on a surface thereof; and

simultaneously delivering a plurality of laser beams to a first plurality of non-contiguous locations on said surface to heat said semiconductor precursor at said non-contiguous locations, and not to substantially heat said semiconductor precursor at other locations.

2. The method claimed in claim 1 and wherein said providing comprises providing a substrate having a layer of amorphous silicon deposited thereon.

3. The method claimed in claim 1 and wherein said simultaneously delivering a plurality of laser beams comprises generating a laser beam and dividing the laser beam into a plurality of sub-beams.

4. The method claimed in claim 3 and further comprising converting the frequency of said laser beam.

5. The method claimed in claim 1 and wherein said delivering a plurality of laser beams comprises inducing said semiconductor precursor to undergo a change in a physical state at said non-contiguous locations, and not to undergo a change in its physical state at other locations.

6. The method claimed in claim 1 and wherein said delivering a plurality of laser beams comprises melting said semiconductor at said non-contiguous locations and not melting said semiconductor precursor at other locations.

7. The method claimed in claim 6 and further comprising cooling said semiconductor precursor.

8. The method claimed in claim 1 and wherein said semiconductor precursor comprises a layer of amorphous silicon and said delivering a plurality of laser beams comprises melting said amorphous silicon at said non-contiguous locations and not melting said amorphous silicon precursor at other locations.

9. The method claimed in claim 6 and further comprising cooling said substrate to crystallize said amorphous silicon at said first plurality of non-contiguous locations.

10. The method claimed in claim 1 and wherein said simultaneously delivering comprises simultaneously delivering said plurality of laser beams to independently selectable non-contiguous locations.

11. The method claimed in claim 1 and further comprising:

simultaneously delivering a plurality of laser beams to a second plurality of non-contiguous locations on said surface to heat said semiconductor precursor at said non-contiguous locations, and not to substantially heat said semiconductor precursor at other locations.

12. The method claimed in claim 11 and wherein said simultaneously delivering a plurality of laser beams to a second plurality of non-contiguous locations comprises simultaneously delivering said plurality of laser beams to independently selectable non-contiguous locations.

13. The method claimed in claim 11 and wherein at least some ones of said second plurality of non-contiguous locations

are different from ones of said first plurality of non-contiguous locations.

14. The method claimed in claim 11 and wherein ones of said first plurality of locations are mutually set apart by a first pitch, and wherein said simultaneously delivering a plurality of laser beams to a second plurality of non-contiguous locations comprises:

delivering said laser beams to said second plurality of non-contiguous locations that are mutually set apart by a second pitch different from said first pitch.

15. The method claimed in claim 1 and wherein said semiconductor precursor comprises amorphous silicon and wherein said delivering comprises delivering a plurality of laser beams to effect a change in a physical state from amorphous silicon to crystalline silicon by heating and then cooling.

16. The method claimed in claim 1 and wherein said semiconductor precursor comprises amorphous silicon and wherein said delivering comprises delivering a plurality of laser beams to effect a change in a physical state from amorphous silicon to poly-silicon by heating and then cooling.

17. The method claimed in claim 1 and wherein said substrate having thin film transistors comprises an in-fabrication flat panel display substrate.

18. The method claimed in claim 1 and further comprising removing portions of said semiconductor not undergoing a change in a physical state.

19. The method claimed in claim 18 and wherein said removing comprises etching said substrate.

20. The method claimed in claim 19 and wherein said etching comprises etching without masking.

21. The method claimed in claim 1 and wherein said delivering said laser beams comprises delivering said laser beams to induce said semiconductor precursor to crystallize into a desired pre-etch crystallized structure at said non-contiguous locations, and further comprising etching said substrate without masking, said desired pre-etch crystallized structure being configured to form a post-etch crystalline structure generally at said non-contiguous locations following said etching and said etching removing said semiconductor precursor from other locations.

22. A method for fabricating a substrate having transistors, comprising:

providing a substrate having a semiconductor precursor deposited thereon;

annealing said semiconductor substrate at a plurality of non-contiguous locations; and

removing said silicon without masking, at least at locations other than at said non-contiguous locations.

23. The method claimed in claim 22 wherein said providing comprises providing a substrate having a layer of amorphous silicon deposited thereon.

24. The method claimed in claim 23 and wherein said annealing comprises annealing said amorphous silicon at said non-contiguous locations to form crystallized silicon thereat, and wherein silicon at locations other than at said non-contiguous locations is not crystallized.

25. The method claimed in claim 23 and wherein said annealing comprises annealing said amorphous silicon at said non-contiguous locations to form poly-silicon crystals thereat, and wherein silicon at locations other than at said non-contiguous locations is not crystallized.

26. The method claimed in claim 22 and wherein said annealing comprises simultaneously delivering a plurality of laser beams to a first plurality of non-contiguous locations.

27. The method claimed in claim 26 and wherein said annealing further comprises subsequently simultaneously delivering a plurality of laser beams to a second plurality of non-contiguous locations, different from said first plurality of non-contiguous locations.

28. The method claimed in claim 22 and wherein said removing comprises etching.

29. The method claimed in claim 28 and wherein said annealing comprises crystallizing said silicon at said non-contiguous locations to form pre-etch crystal formations, and said removing comprises removing at least non-crystallized silicon to leave silicon crystals on said substrate, each silicon crystal having a desired post-etch form.

30. A method for fabricating a flat panel display, comprising:

providing a flat panel display substrate having a semiconductor precursor deposited on a surface thereof; and

simultaneously delivering a plurality of laser beams to a first plurality of non-contiguous locations on said surface to heat said semiconductor precursor at said non-contiguous

locations, and substantially not to heat said semiconductor precursor at other locations.

31. The method claimed in claim 30 and wherein said providing comprises providing a substrate having a layer of amorphous silicon deposited thereon.

32. The method claimed in claim 30 and wherein said simultaneously delivering a plurality of laser beams comprises generating a laser beam and dividing the laser beam into a plurality of sub-beams.

33. The method claimed in claim 32 and further comprising converting a frequency characteristic of said laser beam.

34. The method claimed in claim 30 and wherein said delivering a plurality of laser beams comprises inducing said semiconductor precursor to undergo a change in its physical state at said non-contiguous locations, and not to undergo a change in its physical state at other locations.

35. The method claimed in claim 30 and wherein said delivering a plurality of laser beams comprises melting said semiconductor at said non-contiguous locations and not melting said semiconductor precursor at other locations.

36. The method claimed in claim 35 and further comprising cooling said semiconductor precursor.

37. The method claimed in claim 30 and wherein said semiconductor precursor comprises a layer of amorphous silicon and said delivering a plurality of laser beams comprises melting said amorphous silicon at said non-contiguous locations and not melting said amorphous silicon precursor at other locations.

38. The method claimed in claim 35 and further comprising cooling said substrate to crystallize said amorphous silicon at said first plurality of non-contiguous locations.

39. The method claimed in claim 30 and wherein said simultaneously delivering comprises simultaneously delivering said plurality of laser beams to independently selectable non-contiguous locations.

40. The method claimed in claim 30 and further comprising:

simultaneously delivering a plurality of laser beams to a second plurality of non-contiguous locations on said surface to induce said semiconductor precursor to undergo a change in its physical state at said second plurality of non-contiguous locations, and not to undergo a change its physical state at other locations.

41. The method claimed in claim 40 and wherein said simultaneously delivering a plurality of laser beams to a second plurality of non-contiguous locations comprises simultaneously delivering said plurality of laser beams to independently selectable non-contiguous locations.

42. The method claimed in claim 40 and wherein at least some ones of said second plurality of non-contiguous locations are different from ones of said first plurality of non-contiguous locations.

43. The method claimed in claim 40 and wherein ones of said first plurality of locations are mutually set apart by a first pitch, and wherein said simultaneously delivering a plurality of laser beams to a second plurality of non-contiguous locations comprises:

delivering said laser beams to said second plurality of non-contiguous locations that are mutually set apart by a second pitch different from said first pitch.

44. The method claimed in claim 30 and wherein said semiconductor precursor comprises amorphous silicon and wherein said delivering comprises delivering a plurality of laser beams to effect a change in a physical state from amorphous silicon to crystalline silicon.

45. The method claimed in claim 30 and wherein said semiconductor precursor comprises amorphous silicon and wherein said delivering comprises delivering a plurality of laser beams to effect a change in a physical state from amorphous silicon to poly-silicon.

46. The method claimed in claim 30 and wherein said flat panel display comprises a liquid crystal diode display.

47. The method claimed in claim 30 and further comprising removing portions of said semiconductor precursor not that are not substantially heated.

48. The method claimed in claim 47 and wherein said removing comprises etching said substrate.

49. The method claimed in claim 48 and wherein said etching comprises etching without masking.

50. The method claimed in claim 30 and wherein said delivering said laser beams comprises delivering said laser beams to induce said semiconductor precursor to crystallize into a desired pre-etch crystallized structure at said non-contiguous locations, and further comprising etching said substrate without

masking, said desired pre-etch crystallized structure being configured to form a post-etch crystalline structure generally at said non-contiguous locations following said etching and said etching removing said semiconductor from other locations.

51. A flat panel display substrate manufactured by a method, comprising:

providing a substrate having a layer of amorphous silicon thereon;

selectively annealing portions of said amorphous silicon with a plurality of independently positionable laser beams to form a multiplicity of non-contiguous poly-silicon crystal deposits;

removing portions of said amorphous silicon which are not annealed; and

forming thin film transistors at selected spatially separated poly-silicon crystal deposits.

52. A system for fabricating a substrate having thin film transistors, comprising:

a multi-beam laser processor receiving a substrate having a semiconductor precursor deposited on a surface thereof and said multi-beam laser processor being operative to simultaneously deliver a plurality of laser beams to a first plurality of non-contiguous locations on said surface to a heat semiconductor precursor thereat, and substantially not to heat said semiconductor precursor at other locations.

53. The system claimed in claim 52 and wherein said multi-beam laser processor comprises a beam positioner associated with each of said laser beams operative to deliver said plurality of laser beams to independently selectable non-contiguous locations.

54. The system claimed in claim 52 wherein said multi-beam laser processor comprises a laser outputting a first laser beam and a beam splitter downstream of the laser operative to split the first laser beam into said plurality of laser beams.

55. The system claimed in claim 52 and further comprising:

a controller operative to selectively reposition at least some beam positioners to deliver said plurality of laser beams to a second plurality of non-contiguous locations.

56. The system claimed in claim 55 and wherein ones of said first plurality of locations are set apart by a first pitch and at least some ones of locations among said second plurality of locations are mutually set apart by a second pitch that is different from said first pitch.

57. A system for fabricating arrays of thin film transistors, comprising:

at least one laser source outputting at least two pulsed laser beams;

at least two laser beam positioners receiving said at least two laser beams and directing said at least two laser beams to impinge at non-contiguous locations on a surface of a substrate comprising non-crystallized semiconductor precursor to heat said non-crystallized semiconductor precursor thereat, and substantially not to heat said semiconductor precursor at other locations.

58. The system claimed in claim 57 and wherein said laser source comprises a non-excimer laser.

59. The system claimed in claim 57 and wherein an average power of said laser beam source is less than 50W.

60. The system claimed in claim 57 and wherein a pulse repetition rate of said laser beam source is greater than about 5KHz.

61. The system claimed in claim 57 and wherein said laser beam source comprises a laser outputting a first laser beam and a beam splitter downstream of said laser operative to split said first laser beam into said at least two laser beams.

62. The system claimed in claim 57 and wherein said at least two beam positioners are operative to independently position said at least two laser beams, each at an independently selectable location.

63. The system claimed in claim 57 and wherein ones of said non-contiguous locations are set apart by a first pitch and comprising:

a controller operative to direct said at least two laser beams to a second plurality of locations, wherein at least some ones of locations among said second plurality of locations are mutually set apart by a second pitch that is different from said first pitch.

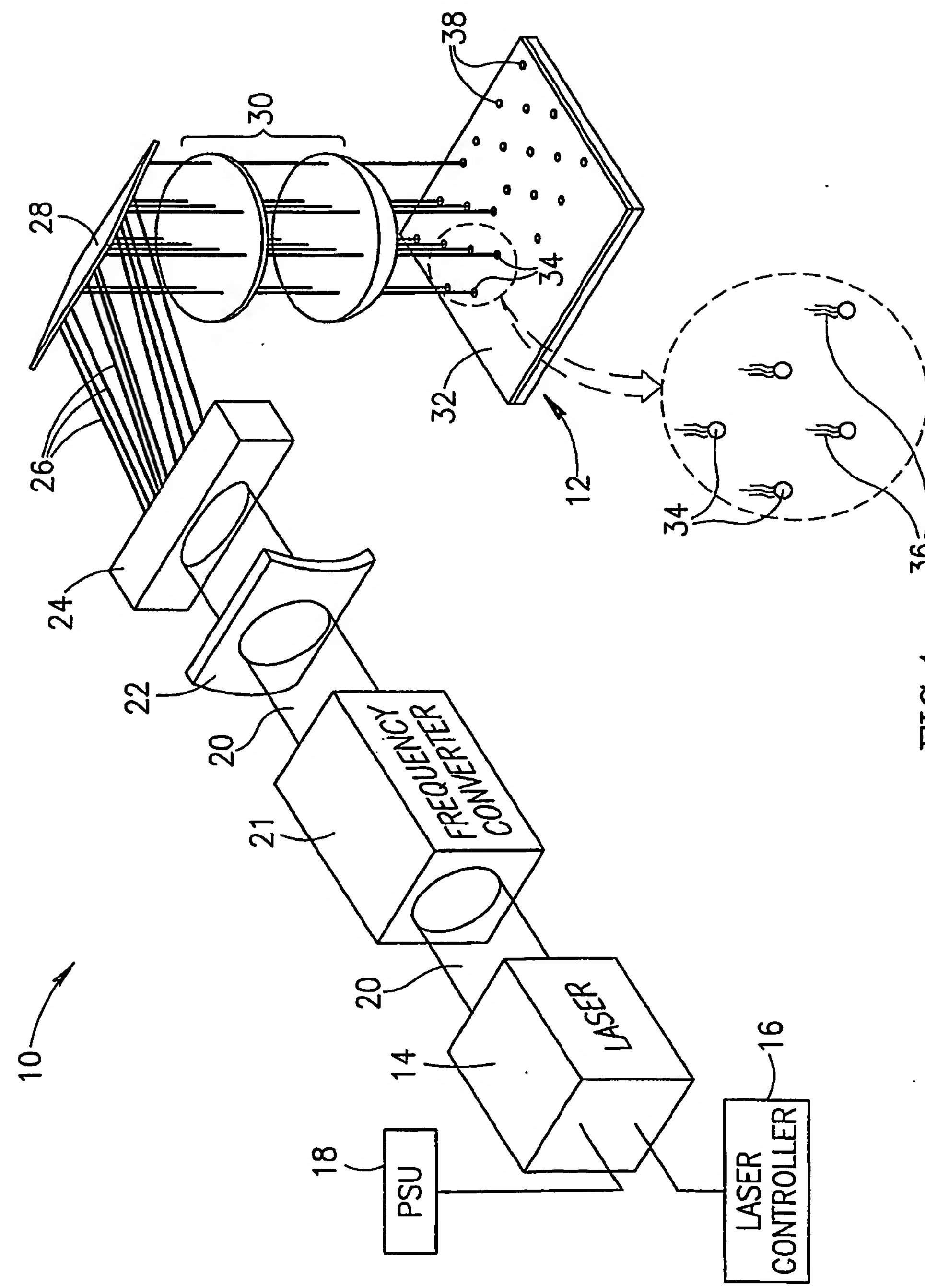
FREQUENCY CONVERTER
LASER
PSU
LASER CONTROLLER
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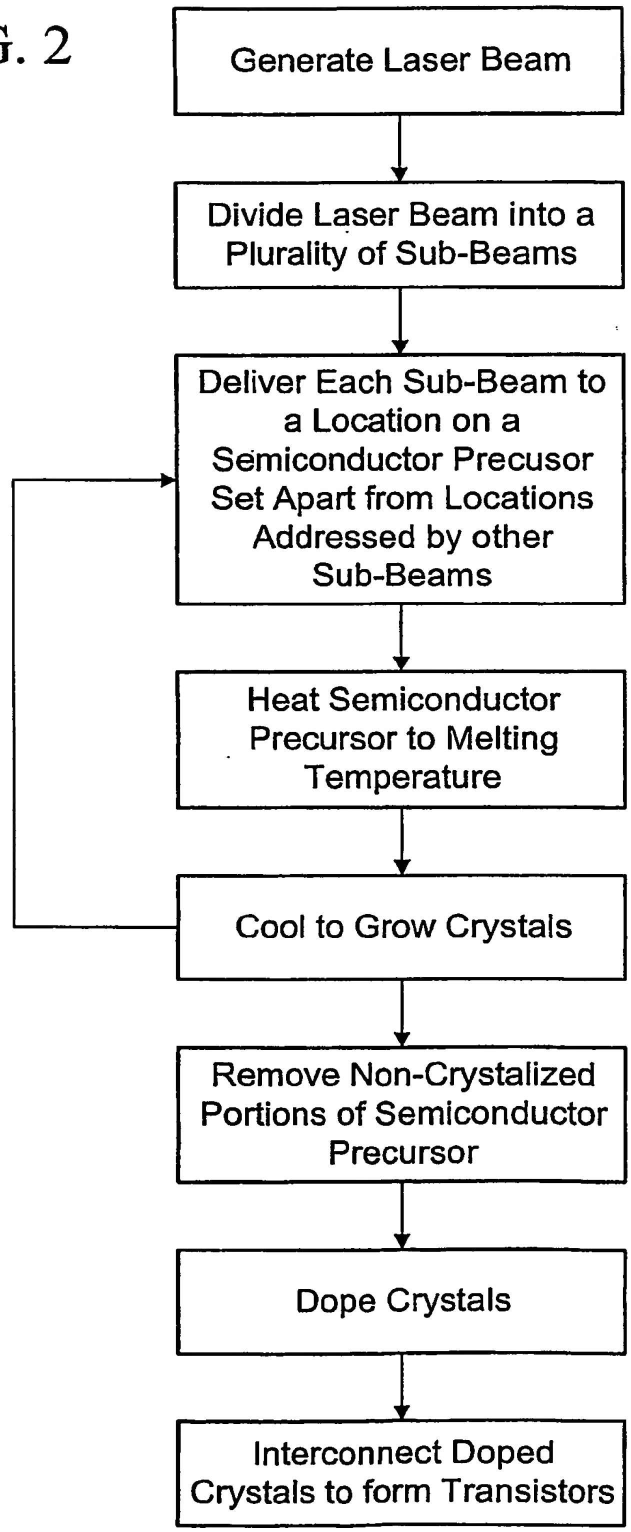
FIG.1

FIG. 2


Generate Laser Beam
Divide Laser Beam into a Plurality of Sub-Beams
Deliver Each Sub-Beam to a Location on a Semiconductor Precusor Set Apart from Locations Addressed by other Sub-Beams
Heat Semiconductor Precursor to Melting Temperature
Cool to Grow Crystals
Remove Non-Crystalized Portions of Semiconductor Precursor
Dope Crystals
Interconnect Doped Crystals to form Transistors

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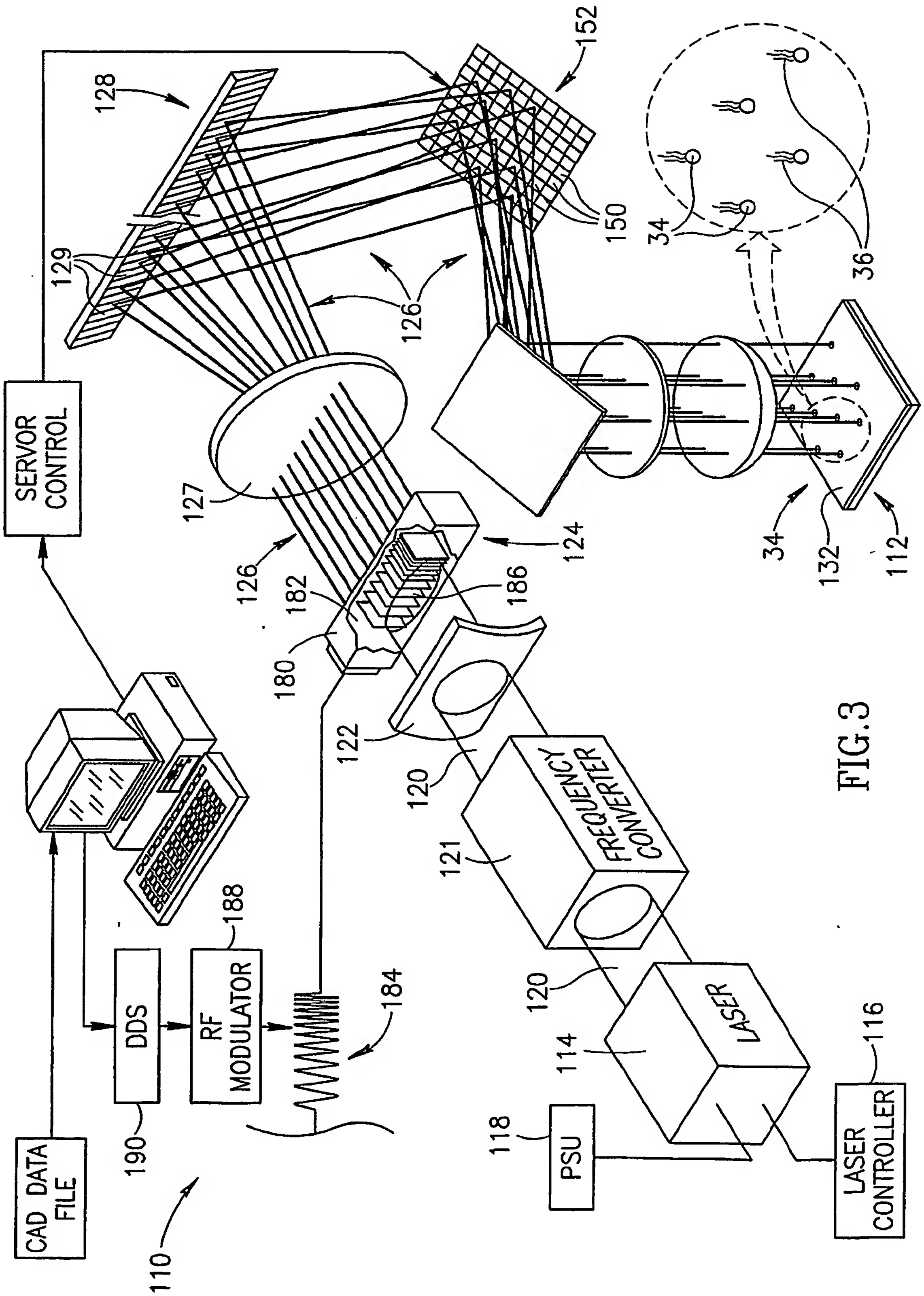
SERVOR CONTROL
CAD DATA FILE
DDS
RF MODULATOR
FREQUENCY CONVERTER
LASER
PSU
LASER CONTROLLER
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120
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122
124
126
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FIG.3

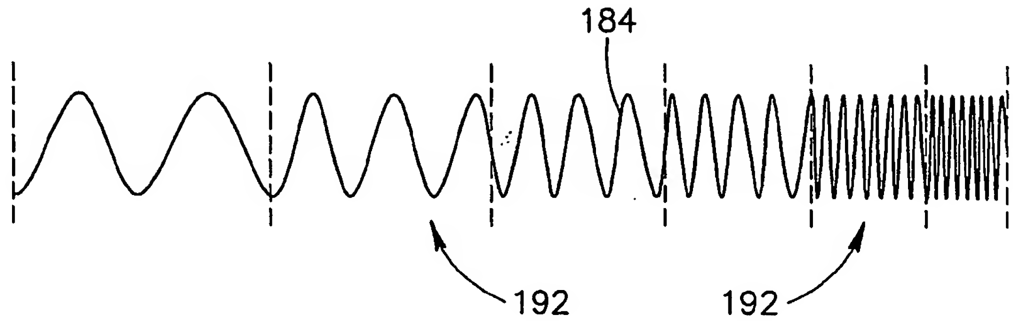

FIG.4

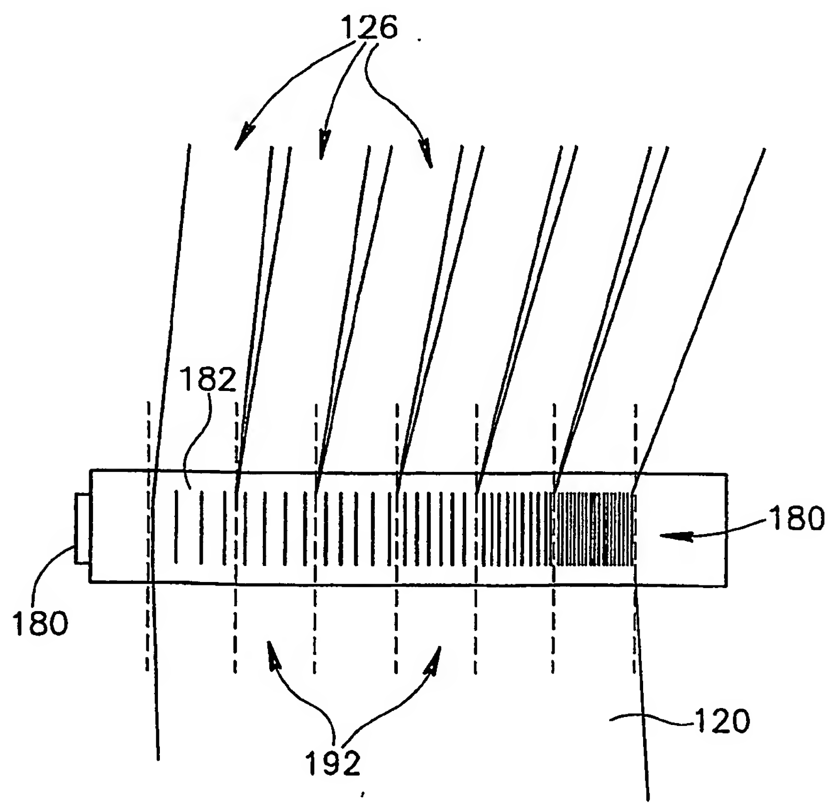

FIG.5

INTERNATIONAL SEARCH REPORT

International application No.
PCT/IL03/00142

A. CLASSIFICATION OF SUBJECT MATTER
IPC(7) : G 02 F 1/136
US CL : 349/43; 313/498.
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
U.S. : 349/43; 313/498.

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
PALM

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EAST

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y,E	US 2002/0030439 A1 (GURVITCH et al.) 14 March 2002, see entire document.	1-63
Y,E	US 2002/0071064 A1 (MOON) 13 June 2002, see entire document.	1-63

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search
28 May 2003 (28.05.2003)

Date of mailing of the international search report
23 JUN 2003

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